

REMARKS / DISCUSSION OF ISSUES

Claims 1-20 are pending in the application.

The Office action rejects claims 1-20 under 35 U.S.C. 102(b) over Abbott (USP 6,006,321). The applicants respectfully traverse this rejection.

Abbott does not teach a programmable connection circuit that receives a set of logic output bits and selectively routes the logic output bits to provide the plurality of output bits that are output to a destination register, based on the output ordering instruction, as claimed in claim 1, upon which claims 2-4 depend.

The Office action asserts that Abbott's transposition circuit 410 of FIG. 4 corresponds to the applicants' claimed second programmable connection. The applicants respectfully disagree with this assertion.

Abbott's circuit 410 is part of Abbott's programmable logic block 114. As illustrated in FIG. 4, Abbott's circuit 410 is included within the reduction network 400, between level one logic circuit 404 and level 2 logic circuit 412. Abbott's transposition circuit 410 alters the bit-order of the output negation circuit 408 to provide an input to the logic circuit 412. That is, Abbott's transposition circuit 412 performs an intermediate re-ordering of bits during the performance of the programmed two-level logic function within logic block 114.

Abbott's circuit 114 does not receive logic output bits from the configurable logic blocks, and does not route these bits to provide the plurality of output bits that are provided to the destination register by a unit output, as specifically claimed in claim 1.

Because Abbott fails to teach the arrangement of elements as claimed, the applicants, the rejection of claims 1-4 under 35 U.S.C. 102(b) over Abbott should be withdrawn.

Abbot does not teach programming a connection circuit subsequent to the logic blocks so as to perform a routing of outputs of the programmable logic blocks to bits of the result data word to which the programmable logic blocks are assigned, as claimed in claim 5. As noted above, Abbott teaches programming a connection circuit to transpose bits between a first logic block and another logic block within the programmable logic block. Accordingly, the rejection of claim 5 under 35 U.S.C. 102(b) over Abbott should be withdrawn.

As noted above, Abbott does not teach selectively coupling bits of an output word to bits of a result word, and outputting the result word to a destination identified in a program instruction, as claimed in claim 6. Accordingly, the rejection of claim 6 under 35 U.S.C. 102(b) over Abbott should be withdrawn.

Abbott does not teach a connection circuit that receives an output word from a programmable logic block in a first output bit order and provides therefrom a word of bits in a second output bit order that is stored in a destination register of a plurality of registers that also provide the input words, as claimed in claim 7, upon which claims 8-12 depend. Accordingly, the rejection of claims 7-12 under 35 U.S.C. 102(b) over Abbott should be withdrawn.

Abbott does not teach a processor that includes a connection circuit that receives the result word from a configurable function circuit and provides an output word for storing in the destination register that includes a plurality of bits that are arranged in a bit order based on the programmed set of configuration data, as claimed in claim 13, upon which claims 14-20 depend. Accordingly, the rejection of claims 13-20 under 35 U.S.C. 102(b) over Abbott should be withdrawn.

In view of the foregoing, the applicants respectfully request that the Examiner withdraw the objection(s) and/or rejection(s) of record, allow all the pending claims, and find the application in condition for allowance. If any points remain in issue that may best be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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